

DisplayPort Technical Overview

Abstract: *This paper provides a technical overview of VESA DisplayPort proposed standard, Version 1, Draft 1. DisplayPort consists of a uni-directional Main Link for transporting isochronous A/V streams from Source device to Sink device and a half-duplex bi-directional AUX CH used for realizing robust plug-n-play ease of use. Both Main Link and AUX CH are made of AC-coupled differential pairs. The Main Link may have 1, 2, or 4 pairs (or lanes), each capable of supporting application bandwidth of 270Mbytes/second while AUX CH has 1 pair. DisplayPort requires no pair for forwarding the clock, thus making the maximum usage of differential pairs. For example, 1680x1050-panel can be supported via a single Main Link lane. Using the handshake via AUX CH, DisplayPort link is properly configured and monitored to realize the robust plug-n-play and ease of use. Source and Sink devices compliant with DisplayPort specification will properly interoperate over 15-meter cable-connector assembly. Connector is compact and has an optional latching feature to avoid undesirable “cable fall-off”. Adopting a layered and modular architecture, DisplayPort can take advantage of advancement of Physical Layer without affecting Link Layer and above. Based on “micro-packet” architecture, DisplayPort is seamlessly extensible for supporting transport of multiple A/V streams and other data types for enabling new display application scenarios.*

Keywords: display; interface; bandwidth; packet transport; industry standard; SERDES; LCD; LVDS, DVI, HDMI, PC, HDTV; VESA; CEA, .

Make-up of DisplayPort

DisplayPort link consists of Main Link, AUX CH, and Hot Plug Detect (HPD) signal line.

As shown in the following diagram, Main Link is a uni-directional, high-bandwidth, and low-latency channel used for transport of isochronous streams such as uncompressed video and audio. AUX CH is a half-duplex bidirectional channel used for link management and device control. The HPD signal also serves as an interrupt request by Sink device.

In addition, the DisplayPort connector for a box-to-box connection has a power pin for powering either a DisplayPort repeater or a DisplayPort-to-Legacy converter.

The table on the next page compares DisplayPort to the existing digital display interfaces used in PC application today.

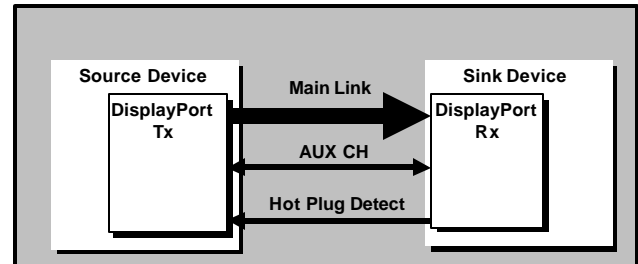


Figure 1. Make-up of DisplayPort

Main Link

Main Link consists of AC-coupled, doubly-terminated differential pairs which are called lanes. AC-coupling allows DisplayPort transmitter and receiver to have different common mode voltages. This facilitates the silicon process migration into deep sub-micron (for example, 65 nm CMOS process) while supporting 0.35 um CMOS process still common for LCD panel TCON (timing controller) chips.

Two link rates are supported: 2.7Gbps and 1.62Gbps per lane. The link rate is decoupled from the pixel rate. The pixel rate is regenerated from the link symbol clock using the time stamp values M and N. The capabilities of the DisplayPort transmitter and receiver, and the quality of the channel (that is, a cable) will determine whether the link rate is set to 2.7Gbps or 1.62Gbps per lane.

The number of lanes of Main Link is 1, 2, or 4 lanes. The number of lanes is decoupled from the pixel bit depth (bits per pixel, or bpp) and component bit depth (bits per component, or bpc). Component bit depths of 6, 8, 10, 12, and 16 are supported with the colorimetry formats of RGB, YCbCr444/422 in DisplayPort proposed standard, Version 1.0, Draft 1, regardless of the number of Main Link lanes.

All lanes carry data: There is no dedicated channel for forwarding clock. Link clock is extracted from the data stream itself that is encoded with ANSI8B/10B coding rule (specified in ANSI X3.230-1994, clause 11).

Source and Sink devices are allowed to support the minimum number of lanes required for their needs. The devices that support 2 lanes are required to support both 1 and 2 lanes, while those that support 4 lanes are required to support 1, 2, and 4 lanes. The external cable that is detachable by an end user is required to support 4 lanes for maximizing the interoperability between Source and Sink devices. When fewer than 4 lanes are enabled, those lanes

with lower lane numbers (starting from Lane 0) must be used.

Excluding the 20% channel coding overhead, DisplayPort Main Link provides for the application bandwidth (also called link symbol rate) as shown below:

Link rate = 2.7Gbps

- 1 lane = 270Mbytes per second
- 2 lanes = 540Mbytes per second
- 4 lanes = 1080Mbytes per second

Link rate = 1.62Gbps

- 1 lane = 162Mbytes per second
- 2 lanes = 324 Mbytes per second
- 4 lanes = 648Mbytes per second

DisplayPort devices may freely trade pixel bit depths with resolution and frame rate of a stream within the available bandwidth. Examples are shown below.

Over 4 lanes

- 12-bpc YCbCr444 (36 bpp), 1920x1080p @ 96Hz
- 12-bpc YCbCr422 (24 bpp), 1920x1080p @ 120Hz
- 10-bpc RGB (30 bpp), 2560x1536 @ 60Hz

Over 1 lane

- 10-bpc YCbCr444 (30 bpp), 1920x1080i @60Hz
- 6-bpc RGB (18 bpp), 1680x1050 @60Hz

Audio and other secondary-data packets may be transported during the horizontal and vertical blanking period of the main video stream.

The highest audio bandwidth expected is about 6Mbytes/sec (= 192kSamples/sec * 32 bits/Sample * 8-ch). Transport of this audio stream is supported over DisplayPort link for any of the video formats specified in VESA DMT and CVT timing standards and CEA -861-B standard with minimum lane count and link rate necessary to support the given video format.

Table 1. Comparison of DisplayPort to existing digital display interface standards used in PC applications today

	DisplayPort	LVDS	DVI
No. of high-speed differential pairs	1, 2, or 4 pairs (No clock pairs)	4 pairs for 18-bpp single link, 10 pairs for 24-bpp dual link (1 & 2 clock pair, respectively)	4 pairs for single link, 7 pairs for dual link (1 clock pair)
For 1680x1050 @18bpp	1 pair	4 pairs	4 pairs
For 1600x1200 @30bpp	2 pairs	12 pairs	7 pairs
For 2048x1536 @36bpp	4 pairs	14 pairs	N/A (or two cables)
Bit rate, per pair	2.7Gbits/sec, fixed rate (1.62Gbps option available)	Up to 0.945Gbits/sec	Up to 1.65Gbps
Total raw capacity per 4-differential pairs	10.8Gbits/sec	2.835Gbits/sec	4.95 Gbits/sec.
AC-coupled for process migration	Yes	No	No
Audio support	Yes	None	None
Aux. channels	1Mbps AUX CH, 500us max. latency	None	DDC, No max. latency limit
Channel Coding	ANSI8B/10B (open)	None	TMDS (Proprietary)
Content protection	Philips's DPCP optional	None	HDCP optional
Protocol	Micro-Packet-based; extensible in the future to add features.	Digitized and serialized analog video raster	Digitized and serialized analog video raster
Internal Connection	Included in first release of spec.	De-facto notebook standard	None
Controlling authority	VESA	ANSI standard	Digital Display Working Group

AUX CH

AUX CH consists of an AC-coupled, doubly terminated differential pair. Manchester II coding is used as the channel coding for AUX CH. As is the case with Main Link, clock is extracted from the data stream. AUX CH transaction starts with the transmission of synchronization

pattern (that is, preamble) to synchronize the sending and receiving devices.

AUX CH is half-duplex, bi-directional. Source device is the master and Sink device the slave. As such, all the AUX CH transactions are initiated by Source device. However, Sink device may prompt the initiation of AUX CH transaction by sending an interrupt request (IRQ) to Source

device by toggling HPD signal. This IRQ feature facilitates the support of Remote Control Command support as specified in CEA-931-B standard.

AUX CH provides for 1Mbps of data rate over the supported cable lengths. Furthermore, each transaction takes no more than 500 us (the maximum burst data size = 16 bytes), thus avoids one AUX CH application from starving other applications.

AUX CH syntax is defined in a way that supports seamless support of I2C transaction over AUX CH.

Layered, Modular Architecture

The diagram below shows the layered architecture of DisplayPort.

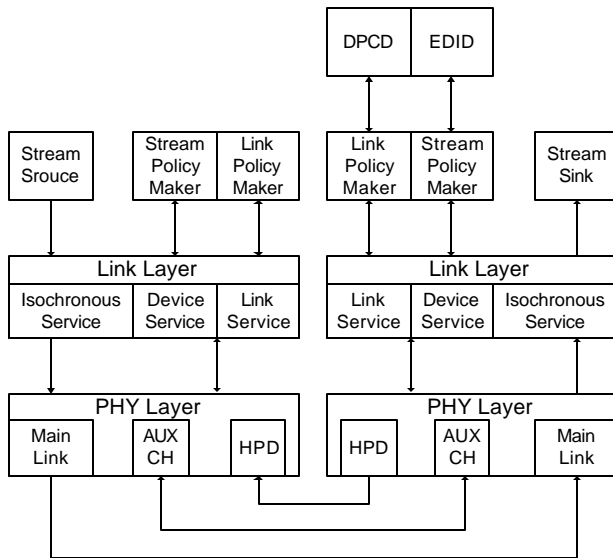


Figure 2. Layered Architecture

In the above diagram DPCD (DisplayPort Configuration Data) in the Sink device describes the capability of the receiver, just as EDID describes that of the Sink device. In addition, DPCD stores the link status information, for example, whether the link is synchronized or not, for link maintenance purpose.

Link and Stream Policy Makers manages the link and the stream, respectively. How they are implemented (state machine, firmware, or system software) is implementation specific. Below Policy Makers and Stream Source/Sink are Link Layer and Physical Layer.

Link Layer

Link Layer provides for the following services:

- Isochronous transport services
- Link and Device Services

Isochronous Transport Services

Isochronous transport services in Source device map the video and audio streams into Main Link with a set of rules,

so that the streams can be properly re-constructed into the original format and time base by Sink device.

The data mapping of a stream to Main Link is devised to facilitate the support of various lane counts. For example, the pixel data is packed and mapped over 4-lane Main Link configurations as follows, regardless of the pixel bit depth and colorimetry format:

Pixel data mapping over 4-lane Main Link

- Pixels 0, 4... : Lane 0,
- Pixels 1, 5... : Lane 1,
- Pixels 2, 6... : Lane 2,
- Pixels 3, 7... : Lane 3

The stream data is packed into “Micro-Packet” which is called “Transport Unit”. The Transport Unit is 64 link symbols long per lane. After the stream data is packed and mapped to Main Link, the packed stream data rate will be equal to or smaller than the link symbol rate of Main Link. When it is smaller, stuffing symbols are inserted.

During the horizontal and vertical blanking period of the main video stream, almost all the link symbols are stuffing symbols, which may be substituted with stream attribute packet (containing the image height, width, etc. of the main video stream) used for regenerating the stream in the Sink device, and optional secondary-data packets such as audio stream packets.

Data integrity is enhanced for the stream attribute packet and the optional secondary-data packets to realize the symbol error rate of $1E-12$. For stream attribute packet, redundancy including majority voting is used. For the optional secondary-data packet, Reed-Solomon-based ECC (error correction coding) is used.

Link and Device Services

Link Service is used for discovering, configuring, and maintaining the link by accessing DPCD via AUX CH.

Upon hot-plug detection, Source device reads the capability of DisplayPort receiver in Sink device and configures the link through Link Training. A proper number of lanes get enabled at a proper link rate with a proper drive current/equalization level, through the handshake between DisplayPort transmitter and receiver via AUX CH. Link Training is designed to be completed within 10 ms.

During normal operation following Link Training, Sink device may notify the link status change, for example, loss of synchronization, by toggling HPD signal, thus, sending an interrupt request. Source device, then checks the link status via AUX CH and takes corrective action. This closed-loop link operation enhances the robustness and interoperability between Source and Sink devices.

Device Service supports device-level applications such as EDID (Extended Display Identification Data) access and MCCC (Monitor Control Command Set) support through AUX CH read/write transactions.

Physical Layer

Physical Layer is divided into two sub-blocks

Logical sub-block

- Scrambling/de-scrambling of data(for Main Link)
- Encoding/Decoding (ANSI8B/10B for Main Link and Manchester II for AUX CH)

Electrical sub-block

- SERDES (Serialization/De-serialization)
- Differential current driving/receiving
- Pre-emphasis/equalization (for Main Link)

DisplayPort Physical Layer specification, when complied, realizes BER (bit error rate) equal to or better than $1E-9$, even over a 15-meter cable. Extensive amount of channel simulation has been run to validate that the eye opening requirement at DisplayPort receiver chip pins can be met over the worst-case (though still within the specification) cable-connector assemblies and PCB traces.

Absence of clock channel and lower count of active lanes help lower the EMI. In addition, scrambling of data symbols prior to ANSI8B/10B encoding eliminates the fixed serial bit pattern, thus reducing the EMI when a video stream with fixed image (for example, many letter H's scrolling on a screen, which is a common test pattern for EMI testing). Furthermore, down-spreading of the link rate (0.5%) is optionally supported for further EMI reduction.

Connectors

Proposed DisplayPort connectors for box-to-box connection are shown below. The connector is compact enough that four of them will fit on a PCI-e bracket. It also fits on the back of an ultra-slim notebook PC.

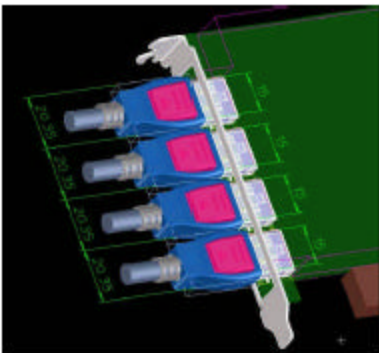


Figure 3. DisplayPort External Connectors

As can be seen in the drawing, proposed DisplayPort connector has an optional latching feature. This feature will prevent the undesirable “cable fall-off” which can be especially problematic with a heavy, long-hop (15 meters long) cable-connector assembly.

As noted earlier, this 20-pin DisplayPort connector has a power pin. The power supply voltage is required to be in the range of +5 ~ +12V, with the minimum current capacity of 500mA. This power is intended to be used to enable an

active dongle with DisplayPort-to-DisplayPort repeater for extending the total cable length or DisplayPort-to-Legacy converter for providing for the interoperability with legacy Sink devices.

VESA DisplayPort proposed standard, Version 1, Draft 1 also specifies a 26-pin, 0.6-mm pitch connector for embedded application. This connector supports four Main Link lanes. How many lanes to populate is implementation specific. Unlike DisplayPort cable-connector assembly for box-to-box connection, it is not required to populate four Main Link lanes.

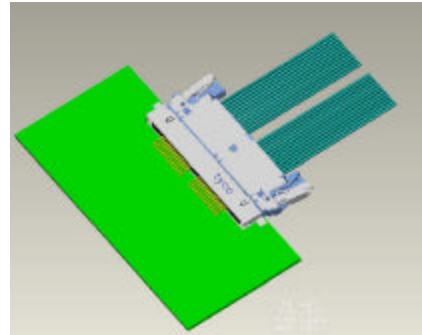


Figure 4. DisplayPort Embedded Connectors

Extensibility

The layered architecture allows DisplayPort to replace Physical Layer in the future while the Link Layer and above stays intact. Speed upgrade to Generation 2, which will double the per-lane bandwidth, is anticipated a few years after the 1st generation of DisplayPort specification. Connector specifications make a speed upgrade to Gen2 possible without requiring the modification to the pin out and form factor.

Furthermore, micro-packet-based transport enables a seamless extension of the DisplayPort specification toward supporting multiple audio-visual streams and other data types. With Gen1 bandwidth, 4-lane Main Link provides for enough bandwidth to transport six HD (either 1080i or 720p) streams simultaneously. Taking advantage of “micro-packet” architecture, packet overhead may be kept to about 10% or less. Furthermore, less than 1Kbytes of buffer may be required.

Not only Main Link, but also AUX CH is extensible. AUX CH data rate may be extended enough to support the transport of captured video and voice from Sink device to Source device.

References

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3. CEA-931-B, Remote Control Command Pass-Through Standard for Home Networking, September, 20.